CLAIMS

What is Claimed Is:

1. A latch circuit comprising:

four or more inverters connected in a loop to hold a signal; and

a plurality of input terminals respectively connected to different nodes, wherein at least one input terminal is used for normal operation of the latch circuit, and at least one input terminal is used for a test operation of the latch circuit.

2. A latch circuit comprising:

four or more inverters connected in a loop to hold a signal; and

a plurality of input terminals and output terminals respectively connected to different nodes, wherein at least one input terminal is used for normal operation of the latch circuit, and at least one input terminal is used for a test operation of the latch circuit.

3. A latch circuit comprising:

four or more inverters connected in a loop to hold a signal; and

a plurality of output terminals respectively connected to different nodes, wherein at least one output terminal is used for normal operation of the latch circuit, and at least one output terminal is used for a test operation of the latch circuit.

4. A latch circuit comprising:

four or more inverters connected in a loop to hold a signal; and

a plurality of input terminals and output terminals respectively connected to different nodes, wherein at least one output terminal is used for normal operation of the latch circuit, and at least one output terminal is used for a test operation of the latch circuit.

5. A latch circuit, comprising:

a first inverter including an input and an output;

a second inverter including an input and an output, the output of the first inverter being connected directly to the input of the second inverter at a first node;

a third inverter including an input and an output, the output of the second inverter being connected directly to the input of the third inverter at a second node; and

a fourth inverter including an input and an output, the output of the third inverter being connected directly to the input of the fourth inverter at a third node,

wherein the output of the fourth inverter is connected directly to the input of the first inverter at a fourth node, and

wherein a first input is connected at the fourth node, a second input is connected at the second node, a first output is connected at the first node and a second output is connected at the third node.

6. A latch circuit as recited in claim 5, wherein the first input and the first output are used during normal operation of the latch circuit, and the second input and the second output are used during a test operation of the latch circuit.

7. A latch circuit as recited in claim 5, wherein the first input is an input address signal, the second input is an input scan signal, the first output is an output address signal and the second output is an output scan signal.

8. A latch circuit, comprising:

a first inverter including an input and an output;

a second inverter including an input and an output, the output of the first inverter being connected to the input of the second inverter;

a third inverter including an input and an output, the output of the second inverter being connected to the input of the third inverter;

a fourth inverter including an input and an output, the output of the third inverter being connected to the input of the fourth inverter at a first node;

a fifth inverter including an input and an output, the output of the fourth inverter being connected to the input of the fifth inverter; and

a sixth inverter including an input and an output, the output of the fifth inverter being connected to the input of the sixth inverter and the output of the sixth inverter being connected to the input of the first inverter at a second node, wherein a first input is connected at the second node, a second input is connected at the first node, a third input is connected at a node between the first node and the second node, a first output is connected at the second node, a second output is connected at the first node and a third output is connected between the first node and the second node.

9. A latch circuit as recited in claim 8, wherein the first input, the second input, the first output and the second output are used during normal operation of the latch circuit, and the third input and third output are used during a test operation of the latch circuit.

10 A latch circuit as recited in claim 8, wherein the first input is an input address signal, the second input is a complement signal of the first input, the third input is an input scan signal, the first output is an output address signal, the second output is a complement of the first output and the third output is an output scan signal.